

# Digital design using VHDL

## Synopsis & Objective of Course

VHDL has been the primary language for electronic product design since its initial ratification by IEEE in 1987. It has been the core of modern synthesis technology for a long time. The course will well equip the trainee with basic concept of design documentation, to design implementation and functional verification. The trainee will have a sound appreciation of sequential statements, simulation & finite state machines too.

## Target Audience

Programmers & designers who wish to gain expertise in hardware language programming.

## Prerequisites

Trainees are expected have to have sound fundamentals in digital design (sequential circuits, flip-flop design etc).

Elementary knowledge of any programming language is helpful.

## Delivery

The training program focuses on hardware development & simulation, so the trainer will help the trainee in getting conceptual understanding of circuit designing & later will demonstrate the various features of simulation.

There will be adequate assignments & a project for hands-on experience.

**Duration : 3 days**

## Course Contents

Day	Topic	Sub topics
Day 1	Introduction to VHDL	VHDL - Overview VHDL - History VHDL - Application Field Concepts of VHDL Abstraction Abstraction levels and VHDL Description of Abstraction Levels Behavioral Description in VHDL Information Content of Abstraction Levels Modularity and Hierarchy
	VHDL Language and Syntax	General Identifier Naming Convention VHDL Structural Elements Declaration of VHDL Objects Entity Architecture Structure Entity Port Modes

		<p>Hierarchical Model Layout  Component Declaration  Component Instantiation  VHDL Communication Model  Signals  Package  Library</p>
<b>Day 2</b>	<b>Data Types</b>	<p>Standard Data Types  Datatype 'time'  Definition of Arrays  'integer' and 'bit' Types  Assignments with Array Types  Types of Assignment for 'bit' Data Types  Concatenation  Aggregates  Slices of Arrays  Extended Data Types  Enumeration Types  BIT Type Issues  Multi-valued Types  IEEE Standard Logic Type  Resolved and Unresolved Types  Std_Logic_1164 Package  Arrays  Multidimensional Arrays  Aggregates and Multidimensional Arrays  Aliases</p>
	<b>Operators</b>	<p>Logical Operators  Logical Operations with Arrays  Shift Operators: Examples  Relational Operators  Comparison Operations with Arrays  Arithmetic Operators</p>
	<b>Sequential Statements</b>	<p>IF &amp; CASE Statement  FOR Loops  Loop Syntax  WAIT Statement  Variables &amp; its usage  Variables vs. Signals  Concurrent Statements  Conditional Signal Assignment  Selected Signal Assignment  Concurrent Statements</p>

<b>Day 3</b>	<b>Subprograms</b>	Parameters and Modes Functions Procedures Subprogram Declaration and Overloading
	<b>Simulations</b>	Sequence of Compilation Example Changes in .. recompile files Simulation Flow Initialization Execution Process Execution Concurrent versus Sequential Execution Signal Update Process Behavior Postponed Processes Delay Models Transport Delay Inertial Delay Test benches Structure of a VHDL Testbench Clock and Reset Generation Stimuli Generation Response Analysis File I/O Example for File I/O
	<b>Finite State Machines in VHDL</b>	One "State" Process Two "State" Processes How Many Processes? State Encoding Extension of Case Statement Extension of Type Declaration Hand Coding FSM: Moore Moore Example Waveform Moore Example FSM: Mealy Mealy Example Waveform Mealy Example Modeling Aspects Registered Output Registered Output Example

**Trainers' Profile**

Corporate Trainer(s) with more than 6 years of experience in embedded development & corporate training in CMM level5 companies.

**Scheduled & On-site Training**

Apart from in-house training programs, comprehensive training can be also provided as per the requirement & will be optimally customized as per the client's needs.

*For training calendar, availability of seats & other details please mail us at [training@sigmasolutions.co.in](mailto:training@sigmasolutions.co.in)*